REMARKS

In the non-final Office Action, the Examiner rejected claims 21, 22, and 26 under 35 U.S.C. § 112, second paragraph, as indefinite; rejected claims 1, 3, 5-9, and 11-18 under 35 U.S.C. § 102(b) as anticipated by Khosrowpour et al. (US Patent No. 5,734,329); rejected claims 10, 19, and 20 under 35 U.S.C. § 103(a) as unpatentable over Khosrowpour et al.; rejected claims 1-3, 5-9, 11-18, 23, 24, and 26-29 under 35 U.S.C. § 102(b) as anticipated by Dickson et al. (U.S. Patent No. 5,644,700); and rejected claim 25 under 35 U.S.C. § 103(a) as unpatentable over Dickson et al. The Examiner objected to claim 4 as dependent upon a rejected base claim, but indicated that it would be allowable if rewritten in independent form to include all of the features of the base claim and any intervening claims. The Examiner indicated that claims 21 and 22 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112.

By this Amendment, Applicant amends claims 1, 9, 10, 17-21, and 23-26 to improve form. Applicant appreciates the Examiner's indication of allowable subject matter, but traverses the Examiner's rejections under 35 U.S.C. §§ 112, 102, and 103 with regard to the claims as now amended. Claims 1-29 remain pending.

At page 1 of the Office Action, the Examiner rejected claims 21, 22, and 26 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. The Examiner alleged that the claims are indefinite because the essential structural cooperative relationships between elements recited in the claim have been omitted (Office Action, page 1). Applicant respectfully traverses the rejection.

Claim 21, for example, recites a bus that includes multiplexed address and data signal lines, a cycle valid signal line, a data/address interval signal line, a read/write signal line, and

parity signal lines. The structural relationship between these different signal lines is present in the claim - they are part of the bus. Applicant has amended claim 21 to make it explicitly clear that the different signal lines are "of the bus." Accordingly, claim 21 is definite, as is claim 22. Withdrawal of the rejection is, therefore, respectfully requested.

Claim 26 recites a control system that includes a bus. The system also includes several means-plus-function elements that perform an operation "on the bus." This provides the necessary structural relationship between the elements. Accordingly, claim 26 is definite. Withdrawal of the rejection is, therefore, respectfully requested.

At pages 1-3 of the Office Action, the Examiner rejected claims 1, 3, 5-9, and 11-18 as allegedly anticipated by Khosrowpour et al. Applicant traverses the rejection.

Amended claim 1, for example, recites a combination of features of a control system that includes a bus, a master device, and a plurality of slave devices. The master device connects to the bus and is configured to commence a bus cycle that includes an address interval and a data interval, provide a destination address on the bus during the address interval, and transmit or receive a command or data during the data interval. The slave devices connect to the bus and are configured to detect commencement of the bus cycle, begin to sample the destination address from the bus one or more clock cycles after commencement of the address interval, and transmit or receive a command or data during the data interval.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. See M.P.E.P. § 2131. Khosrowpour et al. does not disclose or suggest each of the features recited in claim 1. For example, Khosrowpour et al. does not

disclose a bus cycle that includes an address interval and a data interval. Instead, Khosrowpour et al. discloses that a master sends a plurality of data bits that form a command, where each command includes at least one command bit and corresponding address bits (col. 2, lines 31-34).

The Examiner made general allegations regarding the supposed teachings of Khosrowpour et al. (Office Action, page 2). Because these allegations are not directed to the features recited in any of the claims, Applicant finds no need to comment on the accuracy of these allegations.

The Examiner also alleged that "[t]o begin communication, the bus master places the address of the device with which it intends to communicate (the slave) on the bus. All ICs monitor the bus to determine if the master device is sending their address. Only the device with the correct address communicates with the master" (Office Action, page 2). The Examiner's allegation finds no support in the Khosrowpour et al. disclosure and, in fact, Khosrowpour et al. discloses something quite different. At column 2, lines 11-23, Khosrowpour et al. discloses:

> The master transmits several data bits implementing a command, where each bit is combined with clocking pulses. In particular, an initial data pulse incorporates a data bit to initiate a data phase. Then, at least one clock pulse is provided for clocking the data into the slave device. A final reset pulse resets the slave to receive more data bits. This completes transmission of a single bit, where the sequence is repeated for each data bit to be sent. In the preferred embodiment, each command includes a command bit followed by several address or decode bits. The slave preferably includes decode logic to interpret the address for a valid command, and if properly addressed, the command bit is used to perform the desired function.

As evident from this section, Khosrowpour et al. discloses that the master sends a command that includes a command bit followed by several address bits, which is very different from the allegation made by the Examiner.

The Examiner generally identified Figures 1, 1A, 2, and the description thereof in Khosrowpour et al. to support the Examiner's allegations (Office Action, page 2). Nothing in these figures, or the description thereof, supports the Examiner's allegations.

Khosrowpour et al. also does not disclose or suggest a plurality of slave devices that, among other things, begin to sample a destination address from the bus one or more clock cycles after commencement of an address interval, as recited in amended claim 1.

For at least the foregoing reasons, Applicant submits that claim 1 is not anticipated by Khosrowpour et al. Claims 3, 5-9, and 11-16 depend from claim 1 and are, therefore, not anticipated by Khosrowpour et al. for at least the reasons given with regard to claim 1. Claims 3, 5-9, and 11-16 are also not anticipated by Khosrowpour et al. for reasons of their own.

For example, claim 3 recites that the bus includes multiplexed address and data signal lines configured to transport address, data, and commands, a cycle valid signal line configured to indicate a valid bus cycle, and a data/address interval signal line configured to differentiate the data interval from the address interval. Khosrowpour et al. does not disclose or suggest each of these features. For example, Khosrowpour et al. does not disclose or suggest a data/address interval signal line configured to differentiate the data interval from the address interval.

The Examiner alleged that Khosrowpour et al. discloses this feature and cited Figure 1A of Khosrowpour et al. for support (Office Action, page 3). Applicant disagrees.

Khosrowpour et al. describes Figure 1A at column 4, lines 10-20, as:

> FIG. 1A illustrates some of the signals of the SMB 104. In particular, the SMB 104 includes data and clock signals according to the I^2C bus standard by Phillips, and also includes a ground and M_PRESENT signal, along with a plurality of other signals as desired. The M_PRESENT signal is typically used both in systems according to prior art and according to the present invention for signaling to the slave devices 106a-d to

> indicate that the master 102 is present and powered on. The slave devices 106a-d correspondingly power up or down based on the status of the master device 102.

Nowhere in this section, or elsewhere, does Khosrowpour et al. disclose or suggest a data/address interval signal line, as recited in claim 3.

For at least these additional reasons, Applicant submits that claim 3 is not anticipated by Khosrowpour et al.

Claim 13 recites that the master device is further configured to transmit a read-back signal to a destination device, receive a reply to the read-back signal, and determine the integrity of the destination device based on the received reply. Khosrowpour et al. does not disclose or suggest these features. The Examiner did not address these features and, therefore, did not establish a prima facie case of anticipation with regard to claim 13.

For at least these additional reasons, Applicant submits that claim 13 is not anticipated by Khosrowpour et al.

Amended independent claim 17 recites features similar to the features described above with regard to claim 1. Claim 17 is, therefore, not anticipated by Khosrowpour et al. for reasons similar to those given with regard to claim 1. Claim 17 is also not anticipated by Khosrowpour et al. for reasons of its own. For example, claim 17 recites a bus cycle that includes an address interval followed by a data interval. Khosrowpour et al. does not disclose or suggest such a bus cycle. Instead, Khosrowpour et al. discloses a command that includes a command bit followed by several address bits (col. 2, lines 19-20).

For at least these additional reasons, Applicant submits that claim 17 is not anticipated by Khosrowpour et al. Claim 18 depends from claim 17 and is, therefore, not anticipated by Khosrowpour et al. for at least the reasons given with regard to claim 17.

In view of the foregoing, Applicant respectfully requests the reconsideration and withdrawal of the rejection of claims 1, 3, 5-9, and 11-18 under 35 U.S.C. § 102 based on Khosrowpour et al.

At page 4 of the Office Action, the Examiner rejected claims 10, 19, and 20 under 35 U.S.C. § 103(a) as allegedly unpatentable over Khosrowpour et al. Applicant respectfully traverses the rejection.

Claims 10, 19, and 20 variously depend from claim 1 and 17. Claims 10, 19, and 20 are, therefore, patentable over Khosrowpour et al. for at least the reasons given with regard to claims 1 and 17. Claims 10, 19, and 20 are also patentable over Khosrowpour et al. for reasons of their own.

For example, claim 10 recites that a slave device is configured to sample a command or data on the bus 5 clock cycles after commencement of the data interval. Khosrowpour et al. does not disclose or suggest this feature.

The Examiner simply dismissed this feature, alleging that it would have been obvious to one of ordinary skill because "discovering an optimum value of a result effective variable involves only routine skill in the art" (Office Action, page 4). The Examiner's allegation lacks merit. Claim 10 does not relate to discovering an optimum value of a variable, but instead, recites sampling a command or data on a bus 5 clock cycles after commencement of a data interval.

For at least these additional reasons, Applicant submits that claim 10 is patentable over Khosrowpour et al. Similar arguments can be made for claims 19 and 20 because the Examiner's allegation and the Khosrowpour et al. disclosure are similarly deficient.

In view of the foregoing, Applicant respectfully requests the reconsideration and withdrawal of the rejection of claims 10, 19, and 20 under 35 U.S.C. § 103 based on Khosrowpour et al.

At page 3 of the Office Action, the Examiner rejected claims 1-3, 5-9, 11-18, 23, 24, and 26-29 under 35 U.S.C. § 102(b) as allegedly anticipated by Dickson et al. Applicant respectfully traverses the rejection.

Amended claim 1, for example, recites a combination of features of a control system that includes a bus, a master device, and a plurality of slave devices. The master device connects to the bus and is configured to commence a bus cycle that includes an address interval and a data interval, provide a destination address on the bus during the address interval, and transmit or receive a command or data during the data interval. The slave devices connect to the bus and are configured to detect commencement of the bus cycle, begin to sample the destination address from the bus one or more clock cycles after commencement of the address interval, and transmit or receive a command or data during the data interval.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. See M.P.E.P. § 2131. Dickson et al. does not disclose or suggest each of the features recited in claim 1. For example, Dickson et al. does not disclose or suggest a plurality of slave devices that, among other things, begin to sample a destination address from the

bus one or more clock cycles after commencement of an address interval. At column 3, lines 7-26, Dickson et al. discloses the interaction of a master (SBMC) and a slave (SBS) as:

> The SBS 17, the SBMC's 18 and 19, and the SBS spectrum apparatus 21 comprise a maintenance subsystem which performs three major operations (i.e.,protocol). The beginning and ending "handshake", the slave signature packet and the information transfer data packet. With respect to the "handshake", the SBMC 18 or 19 initiates all links to the devices by asserting the INTERRUPT signal and sending a one byte "connect handshake" command. This command contains address data and a command code. The INTERRUPT signal is set until a response is received from the selected device or a connection timeout occurs. The communication link must be terminated with a "disconnect handshake". In order for the link to be successful, the SBS 17 must respond to the SBMC 18 with a "disconnect handshake" before releasing the bus 20 (i.e., disconnects).
>
> The "signature packet" comprises a unique address for each SBS connected to a single SBMC. When a matching address is found between an SBS and the "connect handshake" from the SBMC, the selected SBS responds with a message called the "signature packet".

(see also, col. 3, line 32 - col. 4, line 13). Dickson et al. does not disclose in these sections, or elsewhere, that a slave begins to sample a destination address from a bus one or more clock cycles after commencement of an address interval, as recited in amended claim 1.

For at least these reasons, Applicant submits that claim 1 is not anticipated by Dickson et al. Claims 2, 3, 5-9, and 11-16 depend from claim 1 and are, therefore, not anticipated by Dickson et al. for at least the reasons given with regard to claim 1. Claims 2, 3, 5-9, and 11-16 are also not anticipated by Dickson et al. for reasons of their own.

For example, claim 2 recites that the bus includes a plurality of redundant buses and the master device includes a plurality of redundant master devices, where each of the redundant master devices controls one of the redundant buses. Dickson et al. does not disclose or suggest these features. For example, Dickson et al. does not disclose or suggest redundant buses. Instead, Dickson et al. discloses only a single bus 20 (col. 2, lines 33-36).

The Examiner alleged that Dickson et al. discloses redundant buses and identified items 17 and 20 of Dickson et al. as corresponding to them (Office Action, page 3). Item 17 corresponds to a status bus slave and item 20 corresponds to a bus (col. 2, lines 33-36). Status bus slave 17 is clearly not a bus (see, e.g., Fig. 1).

For at least these additional reasons, Applicant submits that claim 2 is not anticipated by Dickson et al.

Claim 3 recites that the bus includes multiplexed address and data signal lines configured to transport address, data, and commands, a cycle valid signal line configured to indicate a valid bus cycle, and a data/address interval signal line configured to differentiate the data interval from the address interval. Dickson et al. does not disclose or suggest each of these features. For example, Dickson et al. does not disclose or suggest a data/address interval signal line configured to differentiate the data interval from the address interval. The Examiner did not address this feature and, therefore, did not establish a prima facie case of anticipation with regard to claim 3.

For at least these additional reasons, Applicant submits that claim 3 is not anticipated by Dickson et al.

Independent claims 17, 23, and 26 recite features similar to the features described above with regard to claim 1. Claims 17, 23, and 26 are, therefore, not anticipated by Dickson et al. for reasons similar to those given with regard to claim 1. Claims 17, 23, and 26 are also not anticipated by Dickson et al. for reasons of their own.

For example, claim 17 recites, among other things, sampling, by the slave devices, the destination address on the bus a plurality of clock cycles after a start of the address interval. Dickson et al. does not disclose or suggest this feature.

For at least these additional reasons, Applicant submits that claim 17 is not anticipated by Dickson et al.

Claim 26 recites, among other things, means for sampling the data on the bus one or more second clock cycles after a start of the data interval. Dickson et al. does not disclose or suggest this feature. The Examiner did not address this feature and, therefore, did not establish a prima facie case of obviousness with regard to claim 26.

For at least these additional reasons, Applicant submits that claim 26 is not anticipated by Dickson et al.

Claims 18 and 24 depend from claims 17 and 23, respectively. Claims 18 and 24 are, therefore, not anticipated by Dickson et al. for at least the reasons given with regard to claims 17 and 23.

Independent claim 27 recites a combination of features of a multi-master system. The system includes a plurality of redundant buses, a plurality of slave devices connected to the buses, and at least first and second master devices connected to corresponding ones of the buses. The first master device is configured to transmit a read-back signal to a destination device, receive a reply to the read-back signal, and determine the integrity of the destination device based on the received reply.

Dickson et al. does not disclose or suggest each of the features recited in claim 27. For example, Dickson et al. does not disclose or suggest a plurality of redundant buses. Instead, Dickson et al. discloses only a single bus 20 (col. 2, lines 33-36).

The Examiner alleged that Dickson et al. discloses redundant buses and identified items 17 and 20 of Dickson et al. as corresponding to them (Office Action, page 3). Item 17

corresponds to a status bus slave and item 20 corresponds to a bus (col. 2, lines 33-36). Status bus slave 17 is clearly not a bus (see, e.g., Fig. 1).

For at least these reasons, Applicant submits that claim 27 is not anticipated by Dickson et al. Claims 28 and 29 depend from claim 27 and are, therefore, not anticipated by Dickson et al. for at least the reasons given with regard to claim 27.

In view of the foregoing, Applicant respectfully requests the reconsideration and withdrawal of the rejection of claims 1-3, 5-9, 11-18, 23, 24, and 26-29 under 35 U.S.C. § 102 based on Dickson et al.

At page 4 of the Office Action, the Examiner rejected claim 25 under 35 U.S.C. § 103(a) as allegedly unpatentable over Dickson et al. Applicant respectfully traverses the rejection.

Claim 25 depends from claim 23. Claim 25 is, therefore, patentable over Dickson et al. for at least the reasons given with regard to claim 23.

In view of the foregoing, Applicant respectfully requests the reconsideration and withdrawal of the rejection of claim 25 under 35 U.S.C. § 103 based on Dickson et al.

In view of the foregoing amendments and remarks, Applicant respectfully requests the Examiner's reconsideration of the application and the timely allowance of pending claims 1-29.

If the Examiner does not believe that all pending claims are now in condition for allowance, the Examiner is urged to contact the undersigned to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

Paul A. Harrity
Reg. No. 39,574

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11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800